WHAT IS CLAIMED IS:

1. A charge transfer device comprising:

a semiconductor substrate;

a charge transfer path formed in said semiconductor substrate and made of a first conductivity type semiconductor layer;

a plurality of charge transfer electrodes formed near above said charge transfer path; and

a first pulse signal generator circuit for applying either a first pulse signal train for n-phase (n being an integer larger than 1) driving of charges in said charge transfer path to said charge transfer electrodes or a second pulse signal train for (n + 1)-phase driving of charges in said charge transfer path to said charge transfer electrodes.

2. A charge transfer device comprising:

a semiconductor substrate;

a charge transfer path formed in said semiconductor substrate and made of a first conductivity type semiconductor layer;

a plurality of charge transfer electrodes formed near above said charge transfer path; and

a second pulse signal generator circuit for applying either a first pulse signal train for n-phase driving (n being an integer larger than 1) of charges in said charge transfer path to said charge transfer electrodes or a third pulse signal train for (n x m)-phase driving (m being an integer larger than 1) of charges in said charge transfer path to said charge transfer electrodes.

3. A charge transfer device comprising:

a semiconductor substrate;

a charge transfer path formed in said semiconductor substrate and made of a first conductivity type semiconductor layer, said charge transfer path having first barrier layers having a high potential and second well layers having a low potential, disposed alternately;

a plurality of first and second charge transfer electrodes alternately formed near above the first barrier layers and first well layers of said charge transfer path;

a plurality of charge transfer electrode pairs each having adjacent first and second two charge transfer electrodes connected together; and

a third pulse signal generator circuit for applying either a fourth pulse signal train of two-phase for 2-phase driving of charges in said charge transfer path to two charge transfer electrode pairs or a fifth pulse signal train for 2k-phase driving or more of charges in said charge transfer path to the charge transfer electrode pairs.

4. A charge transfer device according to claim 3, further comprising:

a charge storage region formed adjacent to a final stage of the charge transfer electrodes for temporarily storing charges transferred in said charge transfer path; and

a charge detecting region for detecting an amount of charges stored in said charge storage region.

5. A charge transfer device according to claim 4, wherein said charge storage region comprises:

a second barrier layer and a second well layer formed adjacent to each other in said charge transfer path;

a third charge transfer electrode and a fourth charge transfer electrode formed above the second barrier layer and the second well layer; and

a stored charge output pulse generator circuit connected to said third charge transfer electrode and said fourth charge transfer electrode, for generating a stored charge output pulse.

6. A charge transfer device according to claim 3, wherein the second well layer has an electric capacity larger than an electric capacity of the first well layer and the channel transfer device further comprises a floating diffusion region formed adjacent to the second well layer for detecting an amount of charges transferred from said charge transfer path.

7. A charge transfer device comprising:

a semiconductor substrate;

a charge transfer path formed in said semiconductor substrate and made of a first conductivity type semiconductor layer;

a plurality of charge transfer electrodes formed near above said charge transfer path; and

a first pulse signal generator circuit for applying either a first pulse signal train for n-phase (n being an integer larger than 1) driving of charges in said charge transfer path to said charge transfer electrodes or a second pulse signal train for (n + 1)-phase driving of charges in said charge transfer path to said charge transfer electrodes;

a charge storage region formed adjacent to a final stage of the charge transfer electrodes for temporarily storing charges transferred in said charge transfer path; and

a charge detecting region for detecting an amount of charges stored in said charge storage region.

8. A charge transfer device comprising:

a semiconductor substrate;

a charge transfer path formed in said semiconductor substrate and made of a first conductivity type semiconductor layer;

a plurality of charge transfer electrodes formed near above said charge transfer path; and

a second pulse signal generator circuit for applying either a first pulse signal train for n-phase driving (n being an integer larger than 1) of charges in said charge transfer path to said charge transfer electrodes or a third pulse signal train for (n x m)-phase driving (m being an integer larger than 1) of charges in said charge transfer path to said charge transfer electrodes;

a charge storage region formed adjacent to a final stage of the charge transfer electrodes for temporarily storing charges transferred in said charge transfer path; and

a charge detecting region for detecting an amount of charges stored in said charge storage region.

9. A charge transfer device comprising:

a semiconductor substrate;

a charge transfer path formed in said semiconductor substrate and made of a first conductivity type semiconductor layer, said charge transfer path having first barrier layers and second well layers alternately disposed adjacent to each other;

a plurality of charge transfer electrodes formed adjacent to each other above said charge transfer path;

a second pulse signal generator circuit for applying either a first pulse signal train for n-phase driving (n being an integer larger than 1) of charges in said charge transfer path to said charge transfer electrodes or a third pulse signal train for (n x m)-phase driving (m being an integer larger than 1) of charges in said charge transfer path to said charge transfer electrodes;

a charge storage region formed adjacent to a final stage of the charge transfer electrodes for temporarily storing charges transferred in said charge transfer path; and

a charge detecting region for detecting an amount of charges stored in said charge storage region,

wherein said charge storage region comprises:

a second barrier layer and a second well layer formed adjacent to each other in said charge transfer path;

a third charge transfer electrode and a fourth charge transfer electrode formed above the second barrier layer and the second well layer; and

a stored charge output pulse generator circuit connected to said third charge transfer electrode and said fourth charge transfer electrode, for generating a stored charge output pulse, and

wherein an electric capacity of the second well layer has an electric

capacity by (n x m -3) times or more larger than an electric capacity of the first well.

10. A solid state image pickup device comprising; a semiconductor substrate; a plurality of photoelectric conversion elements regularly disposed in row and column directions on the semiconductor substrate; a plurality of vertical charge transfer paths extending in a vertical direction and each disposed adjacent to each of a plurality of photoelectric conversion element columns regularly disposed in the column direction; a read gate formed between each photoelectric conversion element and a corresponding vertical charge transfer path for transferring charges accumulated in the photoelectric conversion element to the vertical charge transfer path; a horizontal charge transfer path formed at one ends of the plurality of vertical charge transfer paths for transferring charges in a horizontal direction; and an output amplifier for amplifying charges transferred by the horizontal charge transfer path and outputting the amplified charges, the horizontal charge transfer path including: a charge transfer path formed in the semiconductor substrate and made of a first conductivity type semiconductor layer, the charge transfer path having first barrier layers having a high potential and second well layers having a low potential, disposed alternately; a plurality of first and second charge transfer electrodes alternately formed near above the first barrier layers and first well layers of the charge transfer path; a plurality of charge transfer electrode pairs each having adjacent first and second two charge transfer electrodes connected together; and a third pulse signal generator circuit for applying either a fourth pulse signal train of two-phase for 2-phase driving of charges in said charge transfer path to two charge transfer electrode pairs or a fifth pulse signal train for 2k-phase driving or more of charges in the charge transfer path to the charge transfer electrode pairs.

11. A solid state image pickup device comprising; a semiconductor substrate; a plurality of photoelectric conversion elements regularly disposed in row and column directions on the semiconductor substrate; a plurality of vertical charge transfer paths extending in a vertical direction and each disposed adjacent to each of a plurality of photoelectric conversion element columns regularly disposed in the column direction; a read gate formed between each photoelectric conversion element and a corresponding vertical charge transfer path for transferring charges accumulated in the photoelectric conversion element to the vertical charge transfer path; a horizontal charge transfer path formed at one ends of the plurality of vertical charge transfer paths for storing charges in first well layers and transferring stored charges in a horizontal direction; and an output amplifier for amplifying charges transferred by the horizontal charge transfer path and outputting the amplified charges, the horizontal charge transfer path including: a first conductivity type semiconductor layer formed in the semiconductor substrate; a plurality of charge transfer electrodes formed adjacent to each other above the horizontal charge transfer path; a second pulse signal generator circuit for applying either a fourth first signal train for n-phase driving (n being an integer larger than 1) of charges in said horizontal charge transfer path to the charge transfer electrodes or a third pulse signal train for (n x m)-phase driving or more (m being an integer larger than 1) of charges in the horizontal charge transfer path to the charge transfer electrodes; a charge storage region formed adjacent to a final stage of the charge transfer electrodes for temporarily storing charges transferred in the horizontal charge transfer path; and a charge detecting region for detecting an amount of charges stored in the charge storage region, the charge storage region including: a second barrier layer and a second well layer formed adjacent to each

other in said charge transfer path; a third charge transfer electrode and a fourth charge transfer electrode formed above the second barrier layer and the second well layer; and a stored charge output pulse generator circuit connected to the third and fourth charge transfer electrodes, for generating a stored charge output pulse, wherein the second well layer has an electric capacity by (n x m - 3) times or more than an electric capacity of the first well layer.

12. A method of reading a solid state image pickup device, the solid state image pickup device including: a semiconductor substrate; a plurality of photoelectric conversion elements regularly disposed in row and column directions on the semiconductor substrate; a plurality of vertical charge transfer paths extending in a vertical direction and each disposed adjacent to each of a plurality of photoelectric conversion element columns regularly disposed in the column direction; a read gate formed between each photoelectric conversion element and a corresponding vertical charge transfer path for transferring charges accumulated in the photoelectric conversion element to the vertical charge transfer path; a horizontal charge transfer path formed at one ends of the plurality of vertical charge transfer paths for transferring charges in a horizontal direction; and an output amplifier for amplifying charges transferred by the horizontal charge transfer path and outputting the amplified charges, the horizontal charge transfer path including: a charge transfer path formed in the semiconductor substrate and made of a first conductivity type semiconductor layer, the charge transfer path having first barrier layers having a high potential and second well layers having a low potential, disposed alternately; a plurality of first and second charge transfer electrodes alternately formed near above the first barrier layers and first well layers of the charge transfer path; a plurality of charge transfer

electrode pairs each having adjacent first and second two charge transfer electrodes connected together; and a third pulse signal generator circuit for applying either a fourth pulse signal train of two-phase for 2-phase driving of charges in said charge transfer path to two charge transfer electrode pairs or a fifth pulse signal train for 2k-phase driving or more of charges in the charge transfer path to the charge transfer electrode pairs, the method comprising:

either a step of, when charges accumulated in all photoelectric conversion elements are read, transferring charges in the horizontal charge transfer path by a two-phase drive method; or

a step of executing a 1/k horizontal thinning operation by selectively reading charges from photoelectric conversion elements adjacent in the horizontal direction of one column per k columns and transferring charges in the horizontal charge transfer path by a 2k-phase drive method.

13. A method of reading a solid state image pickup device, the solid state image pickup device including: a semiconductor substrate; a plurality of photoelectric conversion elements regularly disposed in row and column directions on the semiconductor substrate; a plurality of vertical charge transfer paths extending in a vertical direction and each disposed adjacent to each of a plurality of photoelectric conversion element columns regularly disposed in the column direction; a read gate formed between each photoelectric conversion element and a corresponding vertical charge transfer path for transferring charges accumulated in the photoelectric conversion element to the vertical charge transfer path; a horizontal charge transfer path formed at one ends of the plurality of vertical charge transfer paths for transferring charges in a horizontal direction; and an output amplifier for amplifying

charges transferred by the horizontal charge transfer path and outputting the amplified charges, the horizontal charge transfer path including: a charge transfer path formed in the semiconductor substrate and made of a first conductivity type semiconductor layer, the charge transfer path having first barrier layers having a high potential and second well layers having a low potential, disposed alternately; a plurality of first and second charge transfer electrodes alternately formed near above the first barrier layers and first well layers of the charge transfer path; a plurality of charge transfer electrode pairs each having adjacent first and second two charge transfer electrodes connected together; and a third pulse signal generator circuit for applying either a fourth pulse signal train of two-phase for 2-phase driving of charges in said charge transfer path to two charge transfer electrode pairs or a fifth pulse signal train for 2k-phase driving or more of charges in the charge transfer path to the charge transfer electrode pairs, the method comprising:

either a step of, when charges accumulated in all photoelectric conversion elements are read, transferring charges in the horizontal charge transfer path by a two-phase drive method; or

a step of 2k-phase driving the horizontal charge transfer path when charges of j columns of photoelectric conversion elements are transferred in the horizontal charge transfer path and read through addition.

14. A method of reading a solid state image pickup device, the solid state image pickup device including: a semiconductor substrate; a plurality of photoelectric conversion elements regularly disposed in row and column directions on the semiconductor substrate; a plurality of vertical charge transfer paths extending in a vertical direction and each disposed adjacent to each of a plurality of photoelectric

conversion element columns regularly disposed in the column direction; a read gate formed between each photoelectric conversion element and a corresponding vertical charge transfer path for transferring charges accumulated in the photoelectric conversion element to the vertical charge transfer path; a horizontal charge transfer path formed at one ends of the plurality of vertical charge transfer paths for storing charges in first well layers and transferring stored charges in a horizontal direction; and an output amplifier for amplifying charges transferred by the horizontal charge transfer path and outputting the amplified charges, the horizontal charge transfer path including: a first conductivity type semiconductor layer formed in the semiconductor substrate; a plurality of charge transfer electrodes formed adjacent to each other above the horizontal charge transfer path; a second pulse signal generator circuit for applying either a fourth first signal train for n-phase driving (n being an integer larger than 1) of charges in said horizontal charge transfer path to the charge transfer electrodes or a third pulse signal train for (n x m)-phase driving or more (m being an integer larger than 1) of charges in the horizontal charge transfer path to the charge transfer electrodes; a charge storage region formed adjacent to a final stage of the charge transfer electrodes for temporarily storing charges transferred in the horizontal charge transfer path; and a charge detecting region for detecting an amount of charges stored in the charge storage region, the charge storage region including: a second barrier layer and a second well layer formed adjacent to each other in said charge transfer path; a third charge transfer electrode and a fourth charge transfer electrode formed above the second barrier layer and the second well layer; and a stored charge output pulse generator circuit connected to the third and fourth charge transfer electrodes, for generating a stored charge output pulse, wherein the second well layer has an electric capacity by (n x m - 3) times or more than an electric

capacity of the first well layer, the method comprising:

a step of transferring charges from the charge storage region to the charge detecting region when charges are stored in the charge storage region (n x m - 3) times or more than an electric capacity of the first well.